

CLAIMS

What is claimed is:

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- 1 1. A computer system comprising:
2 a graphics core; and
3 a unified graphics cache coupled to the graphics core, wherein the unified
4 graphics cache stores texture data, color data and depth data.
- 1 2. The computer system of claim 1 wherein the graphics cache comprises:
2 a texture cache to store texture data; and
3 a color and depth buffer to store the color data and the depth data.
- 1 3. The computer system of claim 1 further comprising:
2 a central processing unit (CPU) core; and
3 a CPU cache coupled to the CPU core.
- 1 4. The computer system of claim 3 further comprising a bus interface
2 coupled to the CPU cache and the graphics cache.
- 1 5. The computer system of claim 1 wherein the graphics core operates
2 according to a tile-based rendering architecture.
- 1 6. The computer system of claim 1 further comprising a main memory
2 coupled to the bus interface.

1 7. The computer system of claim 2 wherein the graphics core amplifies
2 image polygons and renders the polygons into the graphics cache.

1 8. The computer system of claim 7 wherein the amplification of the image
2 polygons are implemented via viewport transformation.

1 9. The computer system of claim 7 wherein the graphics core downsamples
2 the image polygons after the polygons have been rendered.

1 10. The computer system of claim 9 wherein the downsampling of the image
2 polygons are implemented by executing a bit aligned block transfer.

1 11. A method for supersampling an image comprising:
2 receiving polygons of a first tile of the image at a graphics core; and
3 rendering the polygons of the first tile into a unified graphics cache,
4 wherein the unified graphics cache stores texture data, color data and depth data
5 of the image.

1 12. The method of claim 11 further comprising amplifying the polygons after
2 receiving polygons at the graphics core.

1 13. The method of claim 12 wherein the polygons are amplified four times the
2 original size of the image.

1 14. The method of claim 12 wherein the amplification is achieved using
2 viewport transformation.

- 1 15. The method of claim 11 wherein the process of rendering the polygons
2 comprises:
3 setting up the image polygons; and
4 rasterizing pixels within the image polygons.
- 1 16. The method of claim 15 further comprising texturing the pixels within the
2 image polygons.
- 1 17. The method of claim 11 further comprising downsampling the polygons
2 after the polygons have been rendered.
- 1 18. The method of claim 17 wherein the downsampling is achieved by
2 executing a bit aligned block transfer.
- 1 19. The method of claim 11 further comprising:
2 determining whether the unified graphics cache includes more tiles that
3 are to be rendered; and
4 if so, receiving polygons of a second tile of the image at the graphics core;
5 and
6 rendering the polygons of the second tile into the unified graphics cache.
- 1 20. A central processing unit (CPU) comprising:
2 a graphics accelerator; and
3 a unified graphics cache coupled to the graphics accelerator, wherein the
4 unified graphics cache stores texture data, color data and depth data.

[illegible]

- 1 21. The CPU of claim 20 wherein the graphics cache comprises:
2 a texture cache to store texture data; and
3 a color and depth buffer to store the color data and the depth data.
- 1 22. The CPU of claim 20 further comprising:
2 a CPU core; and
3 a CPU cache coupled to the CPU core.
- 1 23. The CPU of claim 22 further comprising a bus interface coupled to the
2 CPU cache and the graphics cache.
- 1 24. The CPU of claim 23 wherein the graphics accelerator operates according
2 to a tile-based rendering architecture.